

What is claimed is:

1 1. A feedback control I/O buffer driven by a system
2 voltage, comprising:

3 an input/output circuit comprising a first PMOS
4 transistor and a first NMOS transistor and having
5 a transmission terminal coupled to an I/O pad,
6 wherein the first PMOS transistor has an N-well
7 region, a gate of the first NMOS transistor
8 receives a first gate control signal, and a drain
9 of the first PMOS transistor serves as the
10 transmission terminal;

11 a P-gate control circuit conveying a second gate control
12 signal to the gate of the first PMOS transistor;

13 a feedback detection device having an input coupled to
14 the transmission terminal to output a feedback
15 signal according to an input voltage at the I/O pad;
16 and

17 a N-well control circuit coupled to the P-gate control
18 circuit to control the voltage level at the N-well
19 region of the first PMOS transistor according to
20 the feedback signal output from the feedback
21 detection device.

1 2. The feedback control I/O buffer as claimed in Claim
2 1, wherein the N-well control circuit adjusts the voltage
3 level at the N-well region of the first PMOS transistor to
4 the voltage level of the input voltage when the input voltage
5 exceeds the system voltage.

1 3. The feedback control I/O buffer as claimed in Claim
2 2, wherein the N-well control circuit adjusts the voltage
3 level at the N-well region of the first PMOS transistor to
4 the system voltage when the input voltage is lower than the
5 system voltage.

1 4. The feedback control I/O buffer as claimed in Claim
2 1, wherein the input/output circuit further comprises a second
3 NMOS transistor having a source and drain coupled to the I/O
4 pad and the drain of the first NMOS transistor respectively,
5 and a gate coupled to the system voltage.

1 5. The feedback control I/O buffer as claimed in Claim
2 4, wherein the N-well control circuit comprises:

3 a second PMOS transistor having a source coupled to the
4 I/O pad, a gate coupled to the system voltage, and
5 a drain coupled to the N-well region of the first
6 PMOS transistor;

7 a third PMOS transistor having a gate coupled to the
8 system voltage, a source coupled to the I/O pad,
9 and a drain;

10 a fourth PMOS transistor having a gate coupled to the
11 drain of the third PMOS transistor, a drain coupled
12 to the system voltage, and a source coupled to the
13 N-well region of the first PMOS transistor;

14 a third NMOS transistor having a gate coupled to the
15 feedback signal from the feedback detection
16 device, and a source coupled to the ground; and

17 a fourth NMOS transistor having a gate coupled to the
18 system voltage, a source coupled to a drain of the

19 third NMOS transistor, and a drain coupled to the
20 gate of the fourth transistor.

1 6. The feedback control I/O buffer as claimed in Claim
2 5, wherein the P-gate control circuit comprises:

3 a transmission gate having a fifth NMOS transistor and
4 a fifth PMOS transistor, the sources of which are
5 coupled to the second gate control signal, the
6 drains of which are coupled to the gate of the first
7 PMOS transistor, and the gates of which are coupled
8 to the system voltage and a drain of the third PMOS
9 transistor respectively; and

10 a sixth PMOS transistor having a gate coupled to the
11 system voltage, a drain coupled to the gate of the
12 first PMOS transistor, and a source coupled to the
13 source of the fourth transistor and the N-well
14 region of the first PMOS transistor.

1 7. The feedback control I/O buffer as claimed in Claim
2 1, wherein the feedback detection device is an inverter.

1 8. The feedback control I/O buffer as claimed in Claim
2 7, wherein the inverter comprises:

3 a sixth NMOS transistor having a source coupled to the
4 ground and a drain coupled to the gate of the third
5 NMOS transistor;

6 a seventh PMOS transistor having a source coupled to the
7 system voltage and a drain coupled to the drain of
8 the sixth NMOS transistor; and

9 a seventh NMOS transistor having a gate coupled to the
10 system voltage, a drain coupled to the I/O pad, and

11 a source coupled to gates of the sixth NMOS
12 transistor and the seventh PMOS transistor.

1 9. An input/output buffer, comprising:
2 a floating N-well;
3 a first NMOS transistor having a gate coupled to a first
4 gate control signal, a source coupled to the
5 ground;
6 a second NMOS transistor having a gate coupled to a system
7 voltage, a source coupled to a drain of the first
8 NMOS transistor and a drain coupled to an I/O pad;
9 an inverter having an input terminal coupled to the I/O
10 pad, and an output terminal;
11 a third NMOS transistor having a gate coupled to the
12 output terminal of the inverter and a source
13 coupled to the ground;
14 a fourth NMOS transistor having a source coupled to the
15 drain of the third NMOS transistor, and a gate
16 coupled to the system voltage;
17 a first PMOS transistor having a source coupled to the
18 system voltage, and a drain coupled to the I/O pad;
19 a second PMOS transistor having a source coupled to the
20 I/O pad, a gate coupled to the system voltage, and
21 a drain coupled to the floating N-well;
22 a third PMOS transistor having a source coupled to I/O
23 pad, a gate coupled to the system voltage, and a
24 drain coupled to a source of the fourth NMOS
25 transistor;
26 a fourth PMOS transistor having a gate coupled the drain
27 of the third PMOS transistor, a drain coupled to

28 the system voltage, and a source coupled to the
29 floating N-well;
30 a transmission gate including a fifth NMOS transistor
31 and a fifth PMOS transistor, the sources of which
32 are coupled to a second gate control signal, the
33 drains of which are coupled to the gate of the first
34 PMOS transistor, and the gates of which are coupled
35 to a drain of the third PMOS transistor and the
36 system voltage respectively;
37 a sixth PMOS transistor having a gate coupled to the
38 system voltage, a drain coupled to the gate of the
39 first PMOS transistor and a source coupled to the
40 floating N-well and the source of the fourth PMOS
41 transistor; wherein the floating N-well is
42 connected to the substrate on which the first to
43 sixth PMOS transistors are formed.

1 10. The input/output buffer as claimed in claim 9,
2 wherein the inverter comprises:
3 a sixth NMOS transistor having a source coupled to the
4 ground and a drain coupled to the gate of the third
5 NMOS transistor;
6 a seventh PMOS transistor having a source coupled to the
7 system voltage and a drain coupled to the drain of
8 the sixth NMOS transistor; and
9 a seventh NMOS transistor having a gate coupled to the
10 system voltage, a drain coupled to the I/O pad, and
11 a source coupled to gates of the sixth NMOS
12 transistor and the seventh PMOS transistor.